

## Teradyne A567 Mixed Signal Test System

### License File:

```
SERVER xxx yyyy 7310
# Teradyne license daemon and feature lines
DAEMON icdterd /image/common/icdterd
FEATURE ENABLE_CPD icdterd 3.000 01-jan-0 1 xxx ""
FEATURE ENABLE_SAM icdterd 3.000 01-jan-0 2 xxx "" yyy
FEATURE TESTER icdterd 3.000 01-jan-0 1 xxx "" yyy
# Sun license daemon and feature lines
DAEMON suntechd /image/common/suntechd
INCREMENT sunpro.c suntechd 4.200 1-jan-00 1 xxx ""
```

### CONFSIM File

```
# Confsim file created on: 04/17/04 07:58:43
# A567 tester
#
#      is a 1 processor system
# Processor 1: 40 MHz sparc (online)
# Terabus is present
# Board ID      879-700-03
# Serial number
#
ADV_MIXSIG_TH 1
BACKPLANE A
CONFIGID 879-959-07
#Slot Type      Num      XptA XptB Name
  2  879-657-01  0    # 5   6  THADS24
  3  000-000-00  0    # 7   8  EMPTY
  4  879-858-35  0    # 9  10  PLFD   CC
  5  000-000-00  0    # 11  12  EMPTY
  6  000-000-00  0    # 13  14  EMPTY
  7  000-000-00  0    # 15  16  EMPTY
  8  879-792-00  0    # 17  18  TIME   CC
 14  000-000-00  0    # 19  20  EMPTY
 15  000-000-00  0    # 21  22  EMPTY
 16  879-858-35  0    # 23  24  PLFD   CC
 17  000-000-00  0    # 25  26  EMPTY
 18  000-000-00  0    # 27  28  EMPTY
 19  000-000-00  0    # 29  30  EMPTY
 20  000-000-00  0    # 31  32  EMPTY
 21  000-000-00  0    # 33  34  EMPTY
 22  000-000-00  0    # 35  36  EMPTY
  1  879-656-00  0    # 0   0  RDC48
 12  949-679-00  0    # 3   3  HUC 200
  9  879-653-00  0    # 0   0  HAC
 10  879-654-00  0    # 0   0  TACH
 11  879-667-00  0    # 0   0  ADV_LINEAR CAL
 13  879-834-01  0    # 0   0  Analog Data Buffer AL
END
```

## Teradyne A567 Mixed Signal Test System

# Up to 4 Precision AC Card Cages are allowed

PRECISION\_AC 1

#Slot	Type	Num	Name
1	879-765-04	0	# PLFDIG
2	879-764-01	0	# PLFSRC
3	879-779-00	0	# 1M SMEM
4	879-765-04	0	# PLFDIG
5	879-764-01	0	# PLFSRC
6	879-779-00	0	# 1M SMEM
7	000-000-00	0	# EMPTY
8	879-781-00	0	# PACS CAGE INT

END

# Up to 8 Universal Backplane/Synch Power Subsystem

# cages are allowed

#

# For the Synch Power Subsystem:

# Slot	Type	Name	Instr1	#	Instr2	#	Ammeter	#
--------	------	------	--------	---	--------	---	---------	---

#

# Instr1 # - instrument connected to the first two matrix lines

# Instr2 # - instrument connected to the last two matrix lines

# Ammeter # - ammeter connection

# to AVOID errors, put NO 0 if no instrument is connected.

#

UB\_SPS\_CAGE 1

# Slot	Type	Num	Name
1	879-802-02	0	# UB_SPS_802
2	517-301-01	0	# UB_MATRIX
3	517-301-01	0	# UB_MATRIX
4	517-301-01	0	# UB_MATRIX
5	517-301-01	0	# UB_MATRIX
6	517-301-01	0	# UB_MATRIX
7	517-301-01	0	# UB_MATRIX
8	517-301-01	0	# UB_MATRIX
9	517-301-01	0	# UB_MATRIX
10	517-301-01	0	# UB_MATRIX
11	517-301-00	0	# UB_APU
12	517-301-00	0	# UB_APU
13	517-301-01	0	# UB_MATRIX
14	879-925-01	0	# UB_60_V_SRC MAT 1
15	879-925-01	0	# UB_60_V_SRC DUT 1
16	879-925-01	0	# UB_60_V_SRC MAT 3
17	879-925-01	0	# UB_60_V_SRC MAT 2
18	879-925-01	0	# UB_60_V_SRC MAT 4
19	879-925-01	0	# UB_60_V_SRC MAT 5
20	879-925-01	0	# UB_60_V_SRC DUT 2
21	879-690-00	0	# UB_ASY
22	517-300-01	0	# UB_TJ300

END

## Teradyne A567 Mixed Signal Test System

```
HSD50_CHAN_CAGE 1
#Slot Type      Num      Name
  1  879-933-51  0      # H50 DMF
  2  879-933-51  0      # H50 DMF
  3  879-933-51  0      # H50 DMF
  4  879-933-51  0      # H50 DMF
  5  879-934-01  0      # H50 MFS
  6  879-933-51  0      # H50 DMF
  7  879-933-51  0      # H50 DMF
  8  879-933-51  0      # H50 DMF
  9  879-933-51  0      # H50 DMF
END
```

```
HSD50_SEQ_CAGE 1
#Slot Type      Num      Name
  2  879-945-01  0      # H50 AFO
  4  879-942-05  0      # H50 SFO
  5  879-934-01  0      # H50 MFS
  6  879-937-02  0      # H50 SCM
  7  879-938-01  0      # H50 DMC
END
```

```
ADV_MIXSIG_TH 1
BACKPLANE B
CONFIGID 879-941-02
#Slot Type      Num      Name
 32  879-935-51  0      # H50 DTH
 33  879-935-51  0      # H50 DTH
 34  879-935-51  0      # H50 DTH
 35  879-935-51  0      # H50 DTH
 38  879-943-01  0      # H50 TDR
 40  879-935-51  0      # H50 DTH
 41  879-935-51  0      # H50 DTH
 42  879-935-51  0      # H50 DTH
 43  879-935-51  0      # H50 DTH
 44  879-936-00  0      # H50 THS
END
```

## Teradyne A567 Mixed Signal Test System

HSD50\_DIG\_SIG\_CAGE 1

#Slot	Type	Num	Name
1	879-953-00	0	# VBF
2	879-939-01	0	# DSI
3	879-745-00	0	# S_MEM
4	879-957-00	0	# DCB
5	879-742-40	0	# C_MEM
6	879-745-00	0	# S_MEM
7	879-957-00	0	# DCB
8	879-742-40	0	# C_MEM
9	879-731-00	0	# CAGE INTR

END

#  
# Time Subsystem

#  
TIME\_SUBSYSTEM

#	Board ID	Name
	879-793-00	# TMS Timer
	879-794-01	# TMS Counter
	879-795-01	# TMS Support

END

#  
# DC Subsystem -  
#  
# SRC <NUM> [1 - 13]  
# (sources 1-5 are MATRIX sources 1-5  
# sources 6-13 are DUT sources 1-8)  
# HCU <NUM> \*[1 - 4]  
# REF HCU <NUM> \*[1 - 4]  
# HVSRC <NUM> \*[1 - 4]  
# PWSRC <NUM> [1 - 4]  
# DATABITS <NUM> - <NUM> [1 - 192]  
#

# \*\* These instruments share the same seven-slot cage -- only one  
# instrument is allowed per slot.

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```
#
DC_SUBSYSTEM
# UBVI 60 1 ( 60V V/I Source in Universal Backplane 1 : slot 14)
# UBVI 60 2 ( 60V V/I Source in Universal Backplane 1 : slot 17)
# UBVI 60 3 ( 60V V/I Source in Universal Backplane 1 : slot 16)
# UBVI 60 4 ( 60V V/I Source in Universal Backplane 1 : slot 18)
# UBVI 60 5 ( 60V V/I Source in Universal Backplane 1 : slot 19)
# UBVI 60 6 ( 60V V/I Source in Universal Backplane 1 : slot 15)
# UBVI 60 7 ( 60V V/I Source in Universal Backplane 1 : slot 20)
SRC 8
SRC 9
DATABITS 1 - 48
```

```
# UB_MATRIX
#
# Testhead 1
# XPTs UB Cage Slot Type
# 1-4 1 2 Matrix
# 5-8 1 3 Matrix
# 9-12 1 4 Matrix
# 13-16 1 5 Matrix
# 17-20 1 6 Matrix
# 21-24 1 7 Matrix
# 25-28 1 8 Matrix
# 29-32 1 9 Matrix
# 33-36 1 10 Matrix
# 37-40 1 11 APU
# 41-44 1 12 APU
# 45-48 1 13 Matrix
END
```

```
#
# Array Processor -
# Legal Types : MC860 array processor
# Legal Sizes : 2, 4, and 16MB
#
ARRAY_PROCESSOR
# Type Size
MC860 4MB
END
```