

I U	Head	MX_config
==	====	Chan
awghr	1	[1.. 2]
cx_crate	1	
di ghr	1	[1.. 2]
di gi tal	1	[1.. 112, 129.. 240]
dpro4	1	[1.. 32]
dpro4_chans	1	[1.. 32]
fx1	1	[1.. 64, 129.. 192]
fx1_cbit	1	[1.. 32]
fx1_faxb	1	[1.. 512]
fx1_hd1	1	[1.. 112, 129.. 240]
fx1_tmbd	1	[1.. 256]
fx1_tmbd_di r	1	[1.. 256]
fx1_tmp	1	[1.. 2]
fx1_tmu	1	[1.. 2]
fxhv	1	[65.. 112, 193.. 240]
hss	1	
hvvi	1	[1.. 8, 65.. 72]
mx_testhead	1	
ovi	1	[1.. 8, 65.. 72]
qfvi	1	[17.. 20, 49.. 52]
rf16_sbc	1	[1.. 16]
ssba	1	[1.. 2]
ssbi	1	[1.. 2]
vi 16b	1	[1.. 32, 129.. 144]
vp	1	
vp_suntc	1	

Crate	Slot	Instrument	Board	Channels
=====	=====	=====	=====	=====
68	17	di gi tal	TH_FACFX	[1.. 512]
100	0	cx_crate	CX_CRATE	[1]
101	0	mx_testhead	MX_TESTHEAD	[1]
101	1	ssba	STEPBUSI I _ADAP_NEW	[1]
101	1	ssbi	STEPBUSI I _ADAP_NEW	[1.. 2]
101	2	ovi	OCTAL_VI	[1.. 8]
101	4	qfvi	QFVI_VI	[17.. 20]
101	6	hvvi	HVVI	[1.. 8]
101	7	vi 16b	HEX_VI B	[17.. 32]
101	8	vi 16b	HEX_VI B	[1.. 16]
101	9	awghr	AWGHR	[1.. 2]
101	12	di ghr	DI_GHR	[1.. 2]
101	13	di gi tal	TH_PECHV	[97.. 112]
101	14	di gi tal	TH_PECHV	[65.. 80]
101	15	di gi tal	TH_PECFX	[33.. 48]
101	16	di gi tal	TH_PECFX	[1.. 16]
101	17	di gi tal	TH_TMBDFX_DILR_TMP_REFCLK	[1.. 128]
101	18	di gi tal	TH_PECFX	[17.. 32]
101	19	di gi tal	TH_PECFX	[49.. 64]
101	20	di gi tal	TH_PECFX	[81.. 96]
101	33	ssba	STEPBUSI I _ADAP_NEW	[2]
101	34	ovi	OCTAL_VI	[65.. 72]
101	36	qfvi	QFVI_VI	[49.. 52]
101	38	hvvi	HVVI	[65.. 72]
101	40	vi 16b	HEX_VI B	[129.. 144]
101	45	di gi tal	TH_PECFX	[225.. 240]
101	46	di gi tal	TH_PECFX	[193.. 208]
101	47	di gi tal	TH_PECFX	[161.. 176]
101	48	di gi tal	TH_PECFX	[129.. 144]
101	49	di gi tal	TH_TMBDFX_DILR_TMP	[129.. 256]
101	50	di gi tal	TH_PECFX	[145.. 160]

101	51	di gi tal	MX_config	[177..192]
101	52	di gi tal	TH_PECFX	[209..224]
			TH_PECHV	

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