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<div class="moz-text-flowed" style="font-family: -moz-fixed"># Configuration for: 97156_2, type: S9000KX_SUN, serial number:
CAL_UPDATE_ASAP_REVISIONS /asap/home_621_p14/rel_6.2.1:/asap/home_622_p02/rel_6.2.2

TCS_VTI_ADDR                0xfe800000

#HS_PINS                     0-79:R2.0;448-1023:R2.1 modified to define the new HSCC pins
HS_PINS                      0-79:R2.0;192-199:R2.0;448-1023:R2.1
MAIN_MEM_SIZE                67108864
SUBR_MEM_SIZE                 4096
CAPTURE_MEM_SIZE             126976
SCAN_MEM_SIZE                 0

TH1_MODEL                    1536
#TH1_PINS                    0-79:R5.0,448-1023:R5.0 modified to define the new HSCC pins
TH1_PINS                      0-79:R5.0,192-199:R5.0,448-1023:R5.0
TH1_CALTREE                   F:R4;S:R4

TH1_DCSS_TYPE                1
TH1_PMU                       1
TH1_DPS                       4
TH1_HCDPS                     "HCDPS0 = VHCDPS5-30;
                              HCDPS1 = VHCDPS5-30;
                              HCDPS2 = VHCDPS5-30;
                              HCDPS3 = VHCDPS5-30"

TH1_HSCC                      192

PMU_EINST                     1

STM_OPTION                    2

HDW_APG                       1
setenv APG_CAPTURE            1
NUM_APGS                       1

TESTER_OPTIONS                HCDPS_OPT + 0 + APG_OPT + 0

TCS_SOCK_BASE                 3000
TCS_SYS_TYPE                  S9000KX_SUN
TCS_SSC_PORT                  /dev/ttyb
TCS_NUM_TESTSITES             1
TH1_SIDES                     1
TH2_SIDES                      0

SI02                           1
TH1A_SIO_PORT                 /dev/ttyc3
TH2A_SIO_PORT                  0

OPIO                           1

TH1A_OPIO_PORT                 0xfe7fff00
TH2A_OPIO_PORT                  0

OIC                            1

TH1A_OIC_PORT                  /dev/ttyc0
TH2A_OIC_PORT                  /dev/ttyc1

setenv SYS_ALIGN_OFFSET       20
setenv SHORTED_TDR_OFFSET     -30
setenv CAL_SHORTED_TDR        1

#setenv APG3_REFRESH_ENABLE 1
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