

Teradyne Catalyst - 0717-8

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#
# Confsim file created on: 04/20/07 19:45:21
#
# Catalyst tester
#
# is a 2 processor system
# Processor 1: 150 MHz sparcs (online)
# Processor 3: 150 MHz sparcs (online)
# Terabus is present
# Board ID 879-700-03
# Serial number
# TCI is present
#
```

CATALYST_TH 1 BACKPLANE A

#Slot	Type	Num	XptA	XptB	Name
2	000-000-00	0	# 23	24	EMPTY
3	000-000-00	0	# 21	22	EMPTY
4	000-000-00	0	# 19	20	EMPTY
5	879-792-01	0	# 17	18	TIME CC
6	000-000-00	0	# 15	16	EMPTY
7	000-000-00	0	# 13	14	EMPTY
8	000-000-00	0	# 11	12	EMPTY
9	000-000-00	0	# 9	10	EMPTY
10	000-000-00	0	# 7	8	EMPTY
11	000-000-00	0	# 5	6	EMPTY
14	000-000-00	0	# 25	26	EMPTY
15	000-000-00	0	# 27	28	EMPTY
16	000-000-00	0	# 29	30	EMPTY
17	000-000-00	0	# 31	32	EMPTY
18	000-000-00	0	# 33	34	EMPTY
19	000-000-00	0	# 35	36	EMPTY
20	000-000-00	0	# 37	38	EMPTY
21	000-000-00	0	# 39	40	EMPTY
22	000-000-00	0	# 41	42	EMPTY
23	000-000-00	0	# 43	44	EMPTY
1	949-669-00	0	# 3	0	HAS (Left HAS LA669-00)
13	949-668-00	0	# 0	0	CATALYST HAC
12	949-667-00	0	# 0	0	DIF
24	949-669-01	0x0195bd2	0	# 4	0 HAS (Right HAS LA669-01)

END

RF_PIPES 1

#	pipe-name	slot	schan	description
	Y15B	7	1	# EMPTY (OSSP)
	Y17B	7	2	# EMPTY (OSSP)
	Y16B	7	3	# EMPTY (OSSP)
	Y18B	7	4	# EMPTY (OSSP)

END

```
#
# Up to 4 Precision AC Card Cages are allowed
#
```

PRECISION_AC 1

#Slot	Type	Num	Name
1	000-000-00	0	# EMPTY
2	000-000-00	0	# EMPTY
3	000-000-00	0	# EMPTY
4	000-000-00	0	# EMPTY

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5 000-000-00 0 # EMPTY
6 000-000-00 0 # EMPTY
7 000-000-00 0 # EMPTY
8 949-671-00 0 # PACS CAGE INT
END

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PRECISION_AC 2

```

#Slot Type Num Name
1 000-000-00 0 # EMPTY
2 000-000-00 0 # EMPTY
3 000-000-00 0 # EMPTY
4 000-000-00 0 # EMPTY
5 000-000-00 0 # EMPTY
6 000-000-00 0 # EMPTY
7 000-000-00 0 # EMPTY
8 949-671-00 0 # PACS CAGE INT
END

```

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#
# Up to 8 Universal Backplane/Synch Power Subsystem
# cages are allowed
#
# For the Synch Power Subsystem:
# Slot Type Name Instr1 # Instr2 # Ammeter #
#
# Instr1 # - instrument connected to the first two matrix lines
# Instr2 # - instrument connected to the last two matrix lines
# Ammeter # - ammeter connection
# to AVOID errors, put NO 0 if no instrument is connected.
#
#

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UB_SPS_CAGE 1

```

# Slot Type Num Name
1 879-802-02 0 # UB_SPS_802
2 517-301-00 0 # UB_APU
3 517-301-00 0 # UB_APU
4 517-301-00 0 # UB_APU
5 517-301-00 0 # UB_APU
6 517-301-00 0 # UB_APU
7 517-301-00 0 # UB_APU
8 517-301-01 0 # UB_MATRIX
9 517-301-01 0 # UB_MATRIX
10 517-301-01 0 # UB_MATRIX
11 517-301-01 0 # UB_MATRIX
12 517-301-01 0 # UB_MATRIX
13 517-301-01 0 # UB_MATRIX
14 879-925-01 0 # UB_60_V_SRC DUT 1
15 879-925-01 0 # UB_60_V_SRC MAT 2
16 879-925-01 0 # UB_60_V_SRC MAT 3
17 879-925-01 0 # UB_60_V_SRC MAT 4
18 879-925-01 0 # UB_60_V_SRC MAT 1
19 879-925-01 0 # UB_60_V_SRC DUT 7
20 879-925-01 0 # UB_60_V_SRC DUT 8
21 879-690-00 0 # UB_ASY
22 517-300-01 0 # UB_TJ300
END

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HSD100_CHAN_CAGE

```

1 Num Fld1 Fld2 Name
#Slot Type Num Fld1 Fld2 # HSD CDM 400
1 949-921-01 0 # HSD CDM 400
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2	949-921-01	0	#	HSD	CDM	400
3	949-921-01	0	#	HSD	CDM	400
4	949-921-01	0	#	HSD	CDM	400
5	949-920-10	0	#	HSD	CSB	
6	949-921-01	0	#	HSD	CDM	400
7	949-921-01	0	#	HSD	CDM	400
8	949-921-01	0	#	HSD	CDM	400
9	949-921-01	0	#	HSD	CDM	400

END

HSD100_CHAN_CAGE 2

#Slot	Type	Num	Fld1	Fld2	Name
1	949-921-01	0			# HSD CDM 400
2	949-921-01	0			# HSD CDM 400
3	949-921-01	0			# HSD CDM 400
4	949-921-01	0			# HSD CDM 400
5	949-820-00	0			# HSD CSB
6	949-921-01	0			# HSD CDM 400
7	949-921-01	0			# HSD CDM 400
8	949-921-01	0			# HSD CDM 400
9	949-921-01	0			# HSD CDM 400

END

HSD100_CHAN_CAGE 3

#Slot	Type	Num	Fld1	Fld2	Name
1	949-921-01	0			# HSD CDM 400
2	949-921-01	0			# HSD CDM 400
3	949-921-01	0			# HSD CDM 400
4	949-921-01	0			# HSD CDM 400
5	949-820-00	0			# HSD CSB
6	949-921-01	0			# HSD CDM 400
7	949-921-01	0			# HSD CDM 400
8	949-921-01	0			# HSD CDM 400
9	949-921-01	0			# HSD CDM 400

END

CATALYST_TH 1
BACKPLANE B

#Slot	Type	Num	Name
25	949-625-00	0	# HSD DTH
26	949-625-00	0	# HSD DTH
27	949-625-00	0	# HSD DTH
28	949-625-00	0	# HSD DTH
29	949-626-10	0	# HSD THS
30	949-625-00	0	# HSD DTH
31	949-625-00	0	# HSD DTH
32	949-625-00	0	# HSD DTH
33	949-625-00	0	# HSD DTH
34	949-625-00	0	# HSD DTH
35	949-625-00	0	# HSD DTH
36	949-625-00	0	# HSD DTH
37	949-625-00	0	# HSD DTH
38	949-626-10	0	# HSD THS
39	949-625-00	0	# HSD DTH
40	949-625-00	0	# HSD DTH
41	949-625-00	0	# HSD DTH
42	949-625-00	0	# HSD DTH
43	949-625-00	0	# HSD DTH
44	949-625-00	0	# HSD DTH
45	949-625-00	0	# HSD DTH

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46 949-625-00 0 # HSD DTH
47 949-626-10 0 # HSD THS
48 949-625-00 0 # HSD DTH
49 949-625-00 0 # HSD DTH
50 949-625-00 0 # HSD DTH
51 949-625-00 0 # HSD DTH
52 949-625-00 0 # HSD DTH
53 949-625-00 0 # HSD DTH
54 949-625-00 0 # HSD DTH
55 949-625-00 0 # HSD DTH
56 949-626-10 0 # HSD THS
57 949-625-00 0 # HSD DTH
58 949-625-00 0 # HSD DTH
59 949-625-00 0 # HSD DTH
60 949-625-00 0 # HSD DTH
61 949-625-00 0 # HSD DTH
62 949-625-00 0 # HSD DTH
63 949-625-00 0 # HSD DTH
64 949-625-00 0 # HSD DTH
65 949-626-00 0 # HSD THS
66 949-625-00 0 # HSD DTH
67 949-625-00 0 # HSD DTH
68 949-625-00 0 # HSD DTH
69 949-625-00 0 # HSD DTH
70 949-625-00 0 # HSD DTH
71 949-625-00 0 # HSD DTH
72 949-625-00 0 # HSD DTH
73 949-625-00 0 # HSD DTH
74 949-626-10 0 # HSD THS
75 949-625-00 0 # HSD DTH
76 949-625-00 0 # HSD DTH
77 949-625-00 0 # HSD DTH
78 949-625-00 0 # HSD DTH
END

```

```

#
# Trigger Switch Yard
#
# Note: The logical slot numbers below correspond to the physical slot
#       numbers only for test systems which contain a TSY card
#       cage. In test systems which contain an SCS/TSY card cage the
#       mapping is:
#

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#       Logical TSY slot (below)    Physical slot
#           1                      ->    2
#           3                      ->    1
#

```

TSY CAGE

```

#Slot Type      Num      Name
1 879-655-02 0 # TSY
2 000-000-00 0 # EMPTY
3 000-000-00 0 # EMPTY
4 000-000-00 0 # EMPTY

```

END

```

#
# Time Subsystem
#
TIME_SUBSYSTEM
# Board ID      Name
879-793-00 # TMS Timer

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879-794-01 # TMS Counter
879-795-01 # TMS Support

END

```
#
# DC Subsystem -
#
#   SRC <NUM>                [1 - 13]
#   (sources 1-5 are MATRIX sources 1-5
#   sources 6-13 are DUT sources 1-8)
#   HCU <NUM>                * [1 - 4]
#   REF HCU <NUM>            * [1 - 4]
#   HVSRC <NUM>              * [1 - 4]
#   PWSRC <NUM>              [1 - 4]
#   DATABITS <NUM> - <NUM>   [1 - 192]
#
# ** These instruments share the same seven-slot cage -- only one
#    instrument is allowed per slot.
#
DC_SUBSYSTEM
# UBVI 60 1 ( 60V V/I Source in Universal Backplane 1 : slot 18)
# UBVI 60 2 ( 60V V/I Source in Universal Backplane 1 : slot 15)
# UBVI 60 3 ( 60V V/I Source in Universal Backplane 1 : slot 16)
# UBVI 60 4 ( 60V V/I Source in Universal Backplane 1 : slot 17)
# UBVI 60 6 ( 60V V/I Source in Universal Backplane 1 : slot 14)
# UBVI 60 12 ( 60V V/I Source in Universal Backplane 1 : slot 19)
# UBVI 60 13 ( 60V V/I Source in Universal Backplane 1 : slot 20)
# DATABITS 1 - 48

# UB_MATRIX
#
# Testhead 1
# XPTs UB Cage Slot Type
# 1-4 1 2 APU
# 5-8 1 3 APU
# 9-12 1 4 APU
# 13-16 1 5 APU
# 17-20 1 6 APU
# 21-24 1 7 APU
# 25-28 1 8 Matrix
# 29-32 1 9 Matrix
# 33-36 1 10 Matrix
# 37-40 1 11 Matrix
# 41-44 1 12 Matrix
# 45-48 1 13 Matrix
END
```